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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,434	12/06/2001	Nobuyo Sugiyama	60188-127	7445

7590 08/01/2003

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/003,434	Applicant(s) SUGIYAMA ET AL.	
	Examin r Kevin Quinto	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12 and 22-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-26* is/are allowed.

6)☒ Claim(s) *2-4,6,10,11,27, and 28* is/are rejected.

7)☒ Claim(s) *5,7-9 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. The examiner notes the error in the Notice of References cited. The incorrect reference is Burr et al. (USPN 5,650,340). The correct reference is Burr et al. (USPN 5,780,912) which was accurately cited within the *Claim Rejections - 35 USC § 102* section.

2. The examiner notes the new title and hereby withdraws the objection to the title.

3. The changes made to claims 3-5, 7, and 8 have been noted by the examiner. The objection (regarding grammar) to these claims is hereby withdrawn.

4. Applicant's arguments filed May 15, 2003 have been fully considered but they are not persuasive.

5. Newly amended claim 2 cannot be rejected under 35 U.S.C. 102(b) as being anticipated by Mizutani. However newly amended claim 2 (as well as claims 10, 11, and 28) can be still be rejected under 35 U.S.C. 102(b) as being anticipated by both Kaya and Burr. In addition, newly amended claim 2 (as well as newly amended claims 3, 4, 6 and claims 10, 11, 27, and 28) can be still be rejected under 35 U.S.C. 102(b) as being anticipated by Hori. The applicant disputes the channel location with regard to the Kaya, Burr, and the Hori references. In the prior Office action, the examiner cited Sedra and Smith, "Microelectronic Circuits," 1991, Saunders College Publishing, 3rd ed., p.968-970. In a non-volatile memory transistor such as the devices disclosed in Kaya, Burr, Hori, as well as Sedra and Smith, the select or control gate functions as

typical gate in a regular enhancement mode MOSFET. This is pointed out on p.968 of the Sedra and Smith reference. When the voltage applied to the select or control gate of a non-volatile memory transistor or the gate in a regular enhancement mode MOSFET is greater than the threshold voltage (for an n-type MOSFET), an inversion layer of mobile electrons is formed at the surface. That is, for an n-type transistor (non-volatile memory or an enhancement mode), an inversion layer or channel is formed by inverting the substrate surface from p-type to n-type. On p. 969 of this reference, it is pointed out that the select or control gate, upon the application of a positive voltage (greater than the drain voltage), *creates an inversion layer or channel at the surface of the substrate* because it creates an electric field in the insulating oxide. The floating gate distinguishes the non-volatile memory transistor from the regular enhancement mode MOSFET in that it changes the threshold voltage of the device depending on whether or not this gate is charged. This however does not affect the purpose of the select or control gate which is to induce a channel. The examiner has included with this Office action an additional reference, Sedra and Smith, "Microelectronic Circuits," 1991, Saunders College Publishing, 3rd ed., p.301-302, which discusses transistor physical operation.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 2, 10, 11, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaya et al. (USPN 5,264,384).

8. In reference to claim 2, Kaya et al. (USPN 5,264,384, hereinafter referred to as the "Kaya" reference) discloses a similar device. Figure 10e of Kaya illustrates a nonvolatile semiconductor memory device with a floating gate (13) formed on a semiconductor region via a first dielectric film (22). There is a control gate (14) capacitively coupled with the floating gate (13) via a second dielectric film (23). There is a source region (11) and a drain region (12) formed in the semiconductor region on side regions of the floating gate (13) and the control gate (14). The end of the drain region (12) facing the source region has an embedded drain region (not labeled, but shown more clearly in figure 10b). It is understood that a channel is formed near the surface of the semiconductor region directly above the embedded drain region such that the channel region reaches the surface of the semiconductor region.

9. In reference to claims 10 and 28, the device of Kaya inherently meets these limitations. Carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to the control gate. Furthermore the drain region creates an electric field so that the carriers injected into the floating gate are subject to an external force which has an element directed from the semiconductor region to the floating gate. This operation is explained in column 1, lines 39-47. Sedra

and Smith, "Microelectronic Circuits," 1991, Saunders College Publishing, 3rd ed., p.969, also explains this operation.

10. With regard to claim 11, the control gate (14) is above the floating gate (13).

11. Claims 2, 10, 11, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Burr et al. (USPN 5,780,912).

12. In reference to claim 2, Burr et al. (USPN 5,780,912, hereinafter referred to as the "Burr" reference) discloses a similar device. Figure 3 of Burr illustrates a nonvolatile semiconductor memory device with a floating gate (54) formed on a semiconductor region via a first dielectric film (40'). There is a control gate (56) capacitively coupled with the floating gate (54) via a second dielectric film (not labeled). There is a source region (36') and a drain region (38') formed in the semiconductor region on side regions of the floating gate (54) and the control gate (56). Although figure 3 shows that there is an embedded impurity region (47') on the source side, Burr makes it clear that this embedded impurity region (47') may also be on the drain side (abstract and claim 1). It is understood that a channel is formed near the surface of the semiconductor region directly above the embedded impurity region (47') such that the channel region reaches the surface of the semiconductor region.

13. In reference to claims 10 and 28, the device of Burr inherently meets these limitations. During programming, the source is held to ground while a voltage is applied to the drain. Carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to the control gate or the drain.

Furthermore the drain region creates an electric field so that the carriers injected into the floating gate are subject to an external force which has an element directed from the semiconductor region to the floating gate. This operation is described by Sedra and Smith, "Microelectronic Circuits," p.968-970.

14. With regard to claim 11, the control gate (56) is above the floating gate (54).

15. Claims 2-4, 6, 10, 11, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hori et al. (Published Japanese Application, Publication No.: JP 11-345888).

16. In reference to claim 2, Hori et al. (Published Japanese Application, Publication No.: JP 11-345888, hereinafter referred to as the "Hori" reference) discloses a similar device. Figure 14 of Hori illustrates a nonvolatile semiconductor memory device with a floating gate (3) formed on a semiconductor region (1) via a first dielectric film (2). There is a control gate (5) capacitively coupled with the floating gate (3) via a second dielectric film (4). There is a source region (11a) and a drain region (11b) formed in the semiconductor region (1) on side regions of the floating gate (3) and the control gate (5). The end of the drain region (11b) facing the source region (11a) has an embedded drain region (12b). It is understood that a channel is formed near the surface of the semiconductor region (1) directly above the embedded drain region (12b) such that the channel region reaches the surface of the semiconductor region.

17. With regard to claim 3, there is an embedded region adjacent an upper area (7b) that is formed in an upper part of said embedded drain region (12b) in the

semiconductor region and has a conduction type (p-type) opposite to that of the drain region (11b, n-type).

18. In reference to claim 4, the embedded region adjacent an upper area (7b) has a concentration of 1×10^{17} to 1×10^{18} cm^{-3} (paragraph 148) while the semiconductor region (1) has a concentration of 5×10^{15} to 5×10^{16} cm^{-3} (paragraph 47).

19. With regard to claim 6, figure 14 shows that the embedded drain region (12b) has the same conduction type as that of the drain region (11b).

20. In reference to claims 10 and 28, the device of Hori inherently meets these limitations. The solution section of Hori makes it clear that the electric field is maximized at the drain side of the device during write mode. Thus carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to the control gate or the drain. Furthermore the drain region creates an electric field so that the carriers injected into the floating gate are subject to an external force which has an element directed from the semiconductor region to the floating gate. Sedra and Smith, "Microelectronic Circuits," 1991, Saunders College Publishing, 3rd ed., p.969, also explains this operation.

21. With regard to claim 11, the control gate (5) is above the floating gate (3).

22. With regard to claim 27, the impurity concentration of the embedded drain (12b) is lower than the impurity concentration of the drain (11b).

Allowable Subject Matter

23. Claims 22-26 are allowed.

24. Claims 5, 7-9, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of a non-volatile semiconductor memory device with an embedded drain (below the top surface of the substrate) with an additional upper embedded portion such that the embedded drain has a concentration which is lower than the additional upper embedded portion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
July 24, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800